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| 09/727,486      | 12/04/2000  | Tomoya Yoneda        | 35C.14973           | 4368             |

5514 7590 06/03/2005

FITZPATRICK CELLA HARPER & SCINTO  
30 ROCKEFELLER PLAZA  
NEW YORK, NY 10112

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| EXAMINER |
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GIBBS, HEATHER D

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| ART UNIT | PAPER NUMBER |
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2622

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/727,486

Applicant(s)

YONEDA ET AL.

Examiner

Heather D. Gibbs

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 24 November 2004.  
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1,2,4-6 and 10-18 is/are pending in the application.  
4a) Of the above claim(s) 3,7-9 and 19-22 is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1,2,4-6,10-14 and 18 is/are rejected.  
7) ☒ Claim(s) 13 and 15-17 is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☒ The drawing(s) filed on 04 December 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☒ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Response to Amendment***

1. The amendment filed on 11/24/04 has been entered and made of record. Claims 1-2,4-6,10-18 are currently pending.

### ***Response to Arguments***

2. Applicant's arguments filed have been fully considered but they are not persuasive. Applicant argues "Miida is not seen as teaching or suggesting contacts that supply a reference voltage to a common well in which the source and drain of a transistor for amplification are formed, the contacts being disposed between the picture elements or within the picture elements." Upon further review, the examiner finds this limitation is taught in Fig 2 and Col 7 Lines 50- Col 8 Line26. Miida teaches of the common well 15 being used for the photo-diode as a region for generating charges when it illuminated with light, and serves on the other hand as a gate region for the transistor. The photo-diode has an impurity-diffused region 17, which is formed integral with a drain diffusion region 17a on the well region 15. The drain diffusion 17a is connected with a drain voltage (VDD) supply line 22.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-2,4-6,10-11,18 are rejected under 35 U.S.C. 102(e) as being anticipated by Miida (US 6,051,857).

Regarding claim 1, which is representative of claim 11, Miida teaches a solid state imaging device of an amplification type, comprising: a plurality of picture elements arranged two-dimensionally (Col 7 Lines 53-61; Fig 2), each picture element comprising: a semiconductor light-receiving region 111 of a first conductivity type (p) serving as a photoelectric conversion element, the light-receiving region being disposed in a common well comprising a semiconductor of a second conductivity type (Col 8 Lines 55-60), and a semiconductor region of the first conductivity type serving as a source and drain of a transistor for amplification, the semiconductor region being disposed in the common well; (Col 7 Lines 66- Col 8 Line 14) and a plurality of contacts for supplying a reference voltage to the common well, the plurality of contacts being disposed between the picture elements or within the picture elements (Col 8 Lines 10-14).

Considering claim 2, Miida teaches wherein the contacts are disposed predetermined intervals (Col 9 Lines 48-56).

Considering claim 4, Miida teaches further comprising a plurality of wirings for supplying the reference voltage, each wiring being connected to a corresponding one of the contacts and being disposed in a row direction or a column direction between the

picture elements or within the picture elements at predetermined intervals (Col 9 Lines 48-56).

Considering claim 5, Miida teaches wherein the contacts are disposed at every n rows of the picture elements and the wirings are disposed at every m columns of the picture elements (Col 9 Lines 48-56)

Considering claim 6, Miida teaches wherein the wirings connected to the contacts are disposed at every m rows of the picture elements and the contacts are disposed at every n columns of the picture elements (Col 9 Lines 48-56).

Regarding claim 10, Miida teaches wherein the contacts are also disposed outside the outermost picture elements of the common well (Col 8 Lines 55-60).

Regarding claim 18, Miida teaches wherein the power source contact is connected to a source or a drain of the selection transistor and supplies the power source voltage to the semiconductor region through the selection transistor for selection (Col 9 Lines 57-67; Col 10 Lines 1-6).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 12,14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miida '857 in view of Kunihiro (JP 58-137243).

Regarding claims 12 and 14, Miida teaches of the solid-state imaging device as taught above in claim 11, but fails to particularly teach wherein one of either the reference voltage contacts or the power source contacts is connected to a wiring arranged at every row or every column of the picture elements and the other of the reference voltage contacts or the power source contacts is connected to a shielding layer having a light-receiving window formed above the wiring arranged at every row or every column of the picture elements.

Kunihiro teaches wherein one of the contact and the contact for the power source is connected to a wiring arranged at predetermined intervals in the picture element array area and the other of the contact and the contact for the power source is connected to a shielding layer having a light-receiving window formed above the wiring (constitution).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Midi's solid-state imaging device in the semiconductor circuit device of Kunihiro. Midi's solid-state imaging device would easily be modified to include the circuit device of Kunihiro as both systems share cumulative features making them additive in nature.

### ***Claim Rejections - 35 USC § 112***

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

8. Claims 18 recites the limitation "the selection transistor" in Page 7, Lines 3 and 4. There is insufficient antecedent basis for this limitation in the claim.

***Allowable Subject Matter***

9. Claims 13,15-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

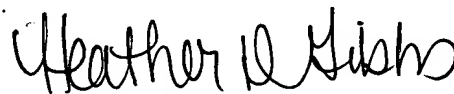
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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather D. Gibbs whose telephone number is 571-272-7404. The examiner can normally be reached on M-Thu 8AM-6PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward L. Coles can be reached on 571-272-7402. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

hdg



Heather D Gibbs  
Examiner  
Art Unit 2622

  
EDWARD COLES

SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600